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A METHOD OF DATA ACQUISITION AND SYSTEM CONTROL THROUGH TIME SHARING OF MIXED INPUTS

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A METHOD OF DATA ACQUISITION
AND
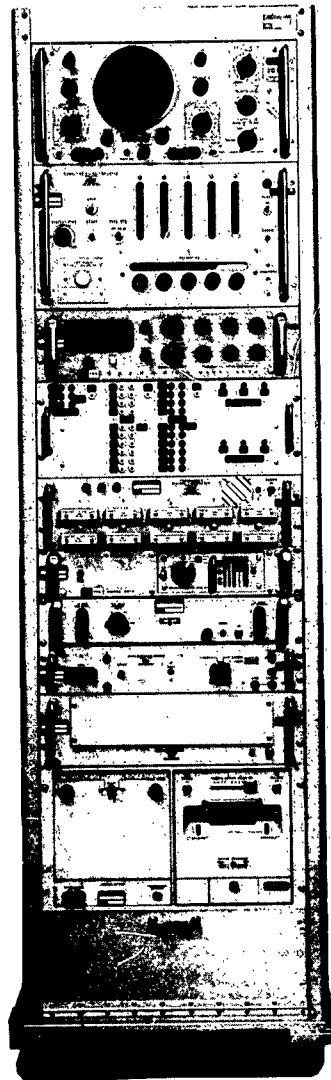SYSTEM CONTROL THROUGH TIME SHARING OF MIXED INPUTS

by

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ACKNOWLEDGEMENT

Data Acquisition and Control System

Fig. I

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I. INTRODUCTION

There are essentially three types of experimental programs under-
taken by engineers. These are: (1) research investigations; (2) devel-
opment programs; and, (3) final product proving tests. No matter what
the purpose, they all have one common requirement — the need to study
the physical behaviour of the product in a controlled but varying
environment. Generally speaking more than one property of the test body
is of interest and it is necessary to observe this at a number of stations.
It is desirable that observations should be made at both internal and ex-
ternal stations and that these observations should be able to be taken
at a location removed from the test site. Thus, in recent years, the
demand for more versatile, remotely readable measuring devices has caused
us to progress, for example, from the simple mechanical extensometer to
the electrical resistance wire gage and from the purely mechanical dial
gage to the variable differential transformer pick up. Instruments of
this type — transducers — have a common property, viz., they transform
some particlular physical behaviour into an electrical signal or change
thereof. Virtually all quantities with which engineers deal can be so
transduced, and the outputs from the devices and varied transducers used
cover the whole spectrum of electrical signals— dc, ac, and frequency.
Thus an inexpensive recording system which can accept any or all of
these types of input, sample the various channels in turn and present
the time dependent data as an accurate numerical quantity is clearly
desirable. The purpose of this thesis is to report the progress made
in the design of such an instrument.

II. THEORY

A logical first consideration in defining the requirements of a data acquisition system is the nature or extent of the problems to be investigated.

In any one investigation several different types of transducers may be employed concurrently to measure the parameters of interest. Such parameters include: strain, force, pressure, displacement, velocity, acceleration, frequency, temperature, radiation flux, and flow rate. At the present state of the art all of these quantities can be transduced to DC, AC, or frequency signals with a high degree of accuracy. The transducer outputs commonly encountered are in the microvolt-millivolt range for DC and AC and 0-100 kilocycles for frequency.

Having outlined the various types of signals to be measured, our next interest lies in the rates of change of these signals — or, expressed in another way, the time interval allowable between monitorings for any one station. The variations in this parameter may well influence still a third: the method of data display. The options available include digital form for high accuracy, analogue form for observation of variation in signal, visual indicators such as lights, and aural signals. The magnitude of the signal, its rate of change, number of events monitored and required accuracy will affect the individual mode or combination of modes selected for the readout.

These then form the parametric skeleton upon which the body of the data acquisition system must be molded.

The conception of our system starts with the signals from the transducers. Since the exclusion of any one of the DC, AC, or frequency modes would sharply reduce the versatility of a general purpose acquisition system, we postulate that all three modes should be acceptable. Further that the system capacity be in the range of 150 to 300 inputs to serve as a useful but not unwieldy machine.

Next, since it is known that the rates of change of the various events to be monitored will not be uniform, it is proposed that variation

in sampling speed for the system and the frequency of sampling any one station be opted by the test engineer.

If the mode of recording which is selected is digital, accuracy and ease in assimilation by the viewer will be achieved. It would, however, be disadvantageous for varying signals. Therefore the adoption of digital printing for primary readout with a secondary capability for analogue display is suggested.

At this point a discussion of controller possibilities should be made. In a truly general purpose machine the incorporation of a controller feature could be of significant assistance to the test conductor. It would enable him to automatically control certain portions of the experiment or possibly the entire test while simultaneously recording the data. Although not all systems operate satisfactorily in any one control method, a controller which provides a sequence of error signals is of fundamental value to most. Further, it would be possible to control several signals with the same device if they are first normalized through a divider network to an appropriate factor of a particular number set in the controller.

In considering a data system which controls several parameters, accepts 3 modes of signals, and has a capacity of several hundred lines, we are dealing with a chain which has a great many parallel links. This is not only costly but also unnecessary in most cases. If time sharing techniques are employed an arrangement of multiple stepping switches can be made to route the various types of signals into distinct channels and to time share the processing components within the channels among the different transducers. Thus we can use a single DC amplifier, a single AC to DC converter, a single DC to frequency converter, a single counter and a single printer as will be explained in detail in Section III. Such a technique, therefore reduces cost and complexity and enables better quality, higher performance components to be adopted for the data processing chain. At the same time uniformity of accuracy is achieved through this single chain concept, and ease of operation is ensured.

III. SYSTEM SYNTHESIS

1. INPUT TO OUTPUT DEVELOPMENT

The synthesis of the time sharing system will be made with reference to Figure 2, System Block Diagram.

Commencing at the left, the DC, AC, and frequency inputs to be measured are connected to the input stations of the scanner in sequential groupings. These stations are sampled on a time shared basis by the scanner wiper arms and the output is fed into the program selector. The program selector channels the information to one of three units — the DC amplifier, the AC-DC converter, or the digital counter — depending upon the instructions it receives from the patch programmer.

If the signal is DC it goes through a DC differential amplifier and the signal is amplified. From there it is sent to a voltage-to-frequency converter where it is converted from a DC voltage into a proportional frequency. If the signal is AC it goes through an AC-DC converter where the signal is attenuated, rectified and smoothed. From the AC-DC converter it goes to the voltage-to-frequency converter. Both the DC amplifier and the AC-DC converter are adjusted in gain for a maximum output of 1 volt which corresponds to a full range 100 kc output of the voltage-to-frequency converter.

After passing through the voltage-to-frequency converter the signal emerges as a frequency. A voltage range of 0-1 volt corresponds to a frequency range of 0-100,000 cps. The signal is then fed to the digital counter. If the input to the scanner is a frequency signal it is sent by the program selector directly to the counter by-passing the amplifier and converters.

The digital counter counts the cycles in incoming frequency signals for a fixed period of time and sends this count to the comparator selector. As in the case of the program selector, the comparator selector is also controlled by the patch programmer. Upon instruction it sends the count from the digital counter either directly to the digital recorder or to both the recorder and to the binary register.
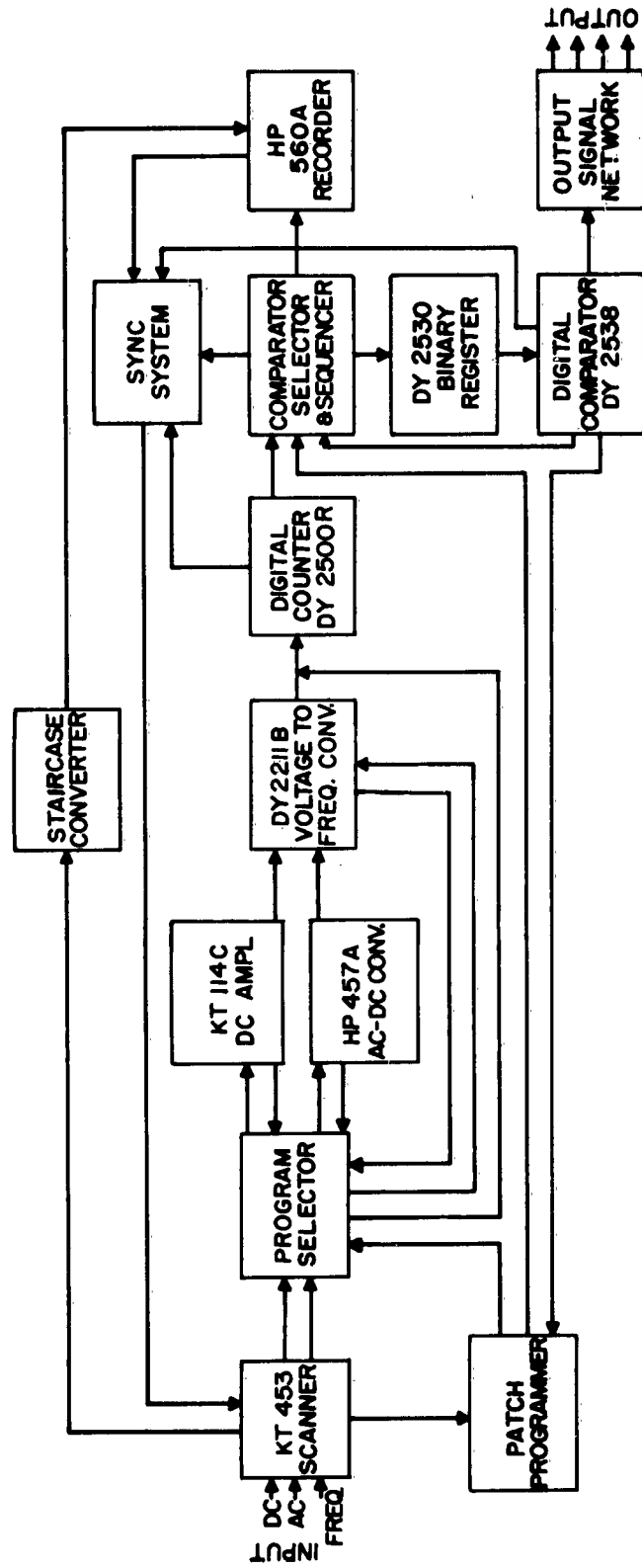
TIME SHARING SYSTEM BLOCK DIAGRAM

FIG. 2

In addition it informs the synchronization system as to the signal route .and hence in which mode the synch system should operate.

If the binary register and comparator are not to be used with the signal, the programmer channels the signal directly to the printer where it is read and printed in 5 digits. Simultaneously with the printing of the value of the signal the printer receives and prints the number of the scanner station from whence the signal came. This station number has been routed through a staircase voltage converter to adapt it for the recorder.

In the case where the signal is to be sent through the digital comparator the programmer tells the comparator selector to "unlock" the binary register. The counter then sends the signal to both the recorder and to the register. The register stores the signal in digital form while the comparator compares it with a preset reference. The error is then found within an increment of tolerance, e.g., less than +5% but higher than +1%. A relay channel peculiar to this particular condition then closes permitting an appropriate correction to be sent to the operation being controlled.

During the above action the digital recorder records the signal received by the comparator and sends a signal to the synch system requesting a new voltage sampling. If the comparator reading is not within the finest preset tolerance limits the scanner will not advance and the sample will be taken from the same station as the previous one. If the comparator is within its finest tolerance limits it allows the scanner to step to a new station. This in effect stops the sharing of other inputs in the data acquisition system until each input being controlled is driven within the prescribed tolerance limits. If it is not desired that the system wait for this action to take place, the operator may manually step the scanner to the next station.

When all of the input signals have been sampled and recorded, the system will either stop or recycle and commence sampling again, depending upon the mode selected by the operator. The maximum rate of sampling in this acquisition system is governed by the recorder whose upper limit is 5 printings per second. Each printing contains eleven columns,

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five of which are the signal; three the channel number of the signal input scanned; and three spares which the operator may use as desired, e.g., time reference.

2. INFORMATION CHANNEL

To prevent additional complexity in scan and switching circuitry, the input signals must be organized according to type into three ordered blocks. The program selector has been designed on this basis. The first block of signals comprise the DC inputs; the second block the AC inputs; and the third, the frequency inputs.

The program selector initially accepts DC inputs. The patch programmer is set up by the operator to switch the program selector to the AC mode at a predesignated input channel number. This number will range from 000 for no DC inputs to 199 for all DC inputs but one. The operator sets the patch programmer for this by jumpering the proper digits jacks and the AC jacks on the patch programmer. For example, if he wishes to switch to AC on the twenty-fifth input, he jumpers 0 in the hundreds, 2 in the tens and 5 in the units to their respective AC jacks. (See Fig. 3.)

When all the AC signals have been sampled the program selector is switched by the patch programmer to the frequency mode. The selection for the frequency mode is made by attaching jumper leads from the appropriate digits jacks to the respective frequency jacks. Upon reaching the desired scanner station the program selector then switches from AC to frequency.

To recycle the scanner to the initial station sampled, the operator sets the last scanner station to be read on the "stop" dials on the scanner. The station desired as the first station to be sampled is similarly dialed on the scanner "start" row.

Any information passed through the scanner, and from there through the remainder of the system, is ultimately recorded. This recording will always be available as a 5 digit readout on printed tape. However, an option exists on the recorder so that any 3 of the 5 digits may be read in analog form on galvanometer or potentiometer type recorders.

HUNDREDS

f_1

0
1   AC
2

TENS

f_2

0
1
2   AC
3
4   AC
5
6
7
8
9

UNITS

f_3

0
1
2
3
4
5   AC
6
7
8
9
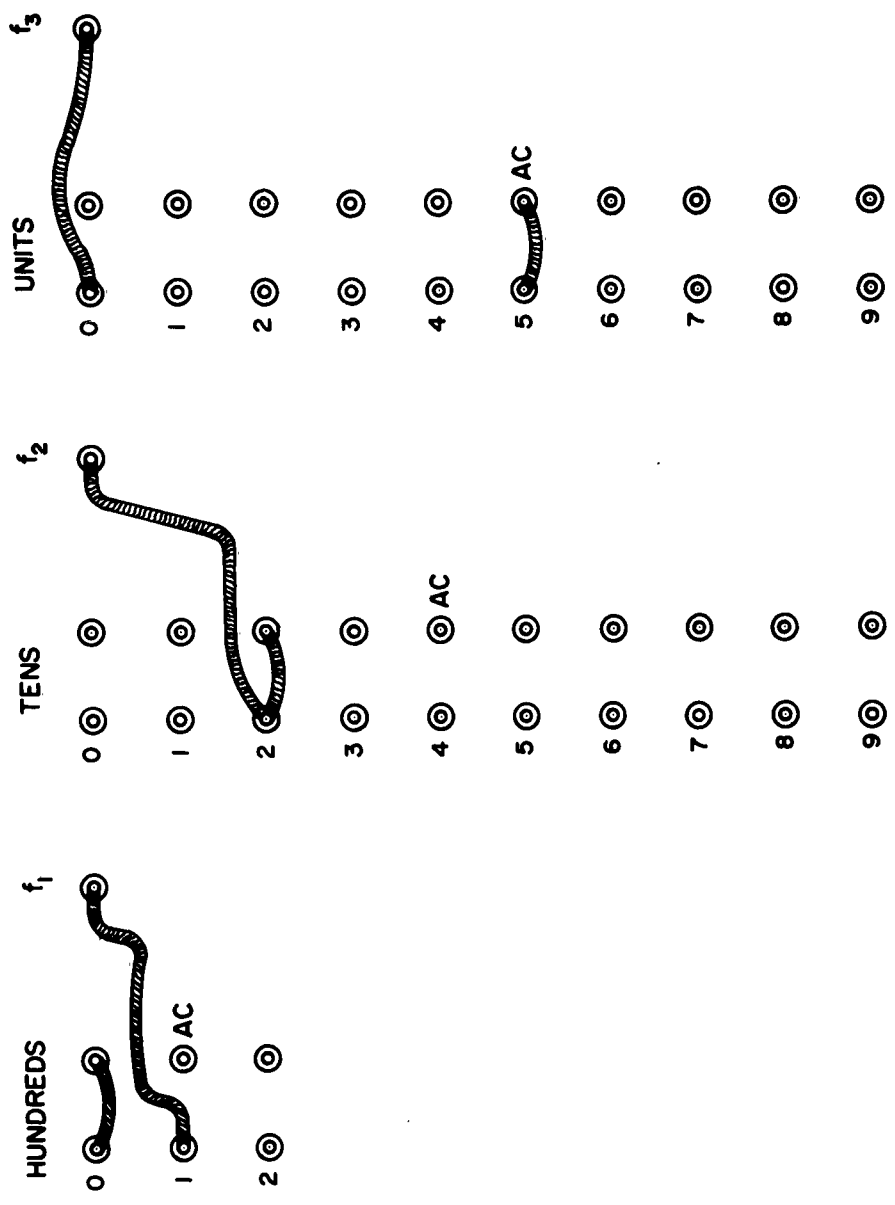
FACE OF PATCH PROGRAMER SHOWING BANANA JACKS AND JUMPER WIRES FOR 025 DC TO AC MODE, 120 AC TO FREQ. MODE.

FIG. 3

3. COMPARATOR OPERATION ·

The comparator is turned on and off through the patch programmer by running jumper wires from the desired digits to the comparitor "on" and "off" jacks. This is done in a manner similar to patching in the stepping from DC to AC.

When the comparator is turned on it compares the incoming signal with a preset number in the comparator. In the system built for this report the number was 1000 (10 millivolts), and all signals to be compared with this standard were normalized to 1000 through precision potentiometers prior to comparison. Upon comparison the comparator notes whether the signal is high, low or within tolerance in five successively refined steps. The flexibility of the comparator output is such that it may be used to simply monitor the error, giving a visual signals, or it may be used as a method of control. In the control mode the comparator operates relays which can provide channels for control instructions from various devices to feed back and correct the monitored system. Alternately, the relay closures provide plus or minus error signals proportional to the category of error, and these voltages in turn may be used to drive controlling devices.

4. SYSTEM SYNCHRONIZATION

In a time shared system it is essential that all components in the data link be logically synchronized in their operation. This is achieved in this acquisition system by slaving all operations to that of the printer when the comparator is not in use and by slaving operations to a combination of the comparator and printer when the comparator is in use.

Using the printer as a basis for synchronization is necessary since the print rate (5 prints/sec) is the limiting factor in rate of scan. When the printer has completed its selection of the proper numbers to print it generates a pulse and thereafter mechanically prints the number. This pulse is used to close a sensitive relay which in turn steps the scanner to the next station to be sampled. During the period that the scanner is stepping from one station to the next, the digital counter

is blocked from counting frequency. This is done by setting the display time for the digital indicator to 0.3 seconds or greater. It takes 0.2 seconds for the printer to complete its cycle and 0.1 second for the scanner to step and make firm contact with the next input terminal.

When the comparator is "on", the pulse generated by the printer is blocked from stepping the scanner unless the input is within the closest tolerance limit on the comparator. In this mode the input is digitized by the digital indicator and printed by the recorder. When the recorder has finished its cycle the indicator takes another reading on the same station, the printer prints it, and the cycle repeats until the comparator output has caused the signal to be driven within the final tolerance limits. When this is achieved and the printer has printed, the comparator programmer steps the scanner to the following station.

IV. SYSTEM COMPONENTS

1. A <u>Kintel 453 M Scanner</u> is the basic time sharing element in the data link. It accepts inputs from the various transducers, and sequentially samples and routes them to the program selector. The scanner is fed through 8 Amphenol connectors. Each connector has 50 gold-plated contacts which are wired to gold-plated stepping switches. The capacity is 200 two-line inputs, half of which are shielded. The switches step on command given either by an external source or an internal timer. The bounds of the scan cycle are determined by selected dial settings.

The scanner can step 10 times per second in its normal configuration. This rate can be doubled by a modification described in the scanner operating instructions; however the system rate is constrained to a maximum of 5 samples per second by the recorder.

2. The <u>Patch Programmer</u> provides the method for stepping the program selector which routes DC, AC and frequency signals to the appropriate link in the data chain. In addition it turns the comparator on and off. The first task is to instruct the program selector where to route a signal. This is done through the patch board. The patch board has banana jacks arranged in hundreds, tens and units. Each jack is connected to a particular pin on the J3 slave station connector of the scanner.

The operator, desiring switching to AC on number 149 for example, would plug a shorted dual banana plug into 1 in the hundreds column, 4 in the tens column, and 9 in the units. These plugs each provide continuity from the scanner J3 plug 6 volt slave station outputs to pin RR on J-3 which is also at 6 volts. (See Figure 7.) So long as the number selected is not read by the scanner the relay "floats" at 6 volts. However when the scanner steps to a number — such as the 1 in 149 — the six volts on the J-3 pin drop out and six volts appear across the hundreds digit patch relay, closing it. When the number 149 appears, all three relays close. A 5 microfarad capacitor is in series with the unit plugs for AC so that the units relay closes only for a moment while the capacitor charges up. This provides a 48 v pulse to the program selector minor
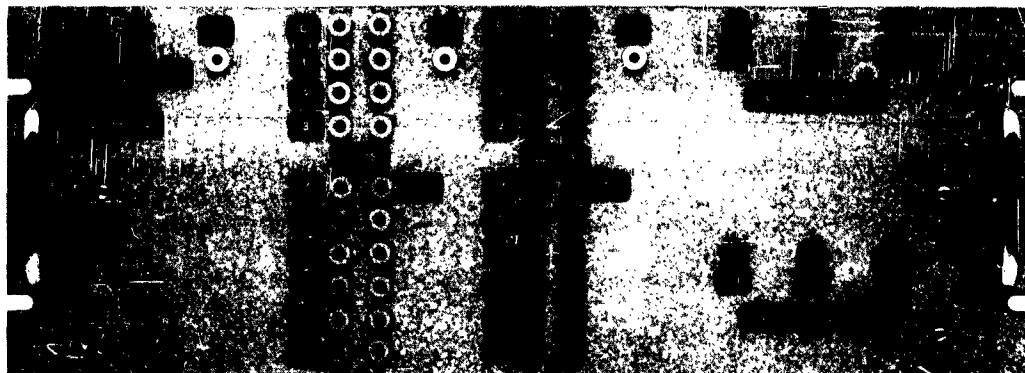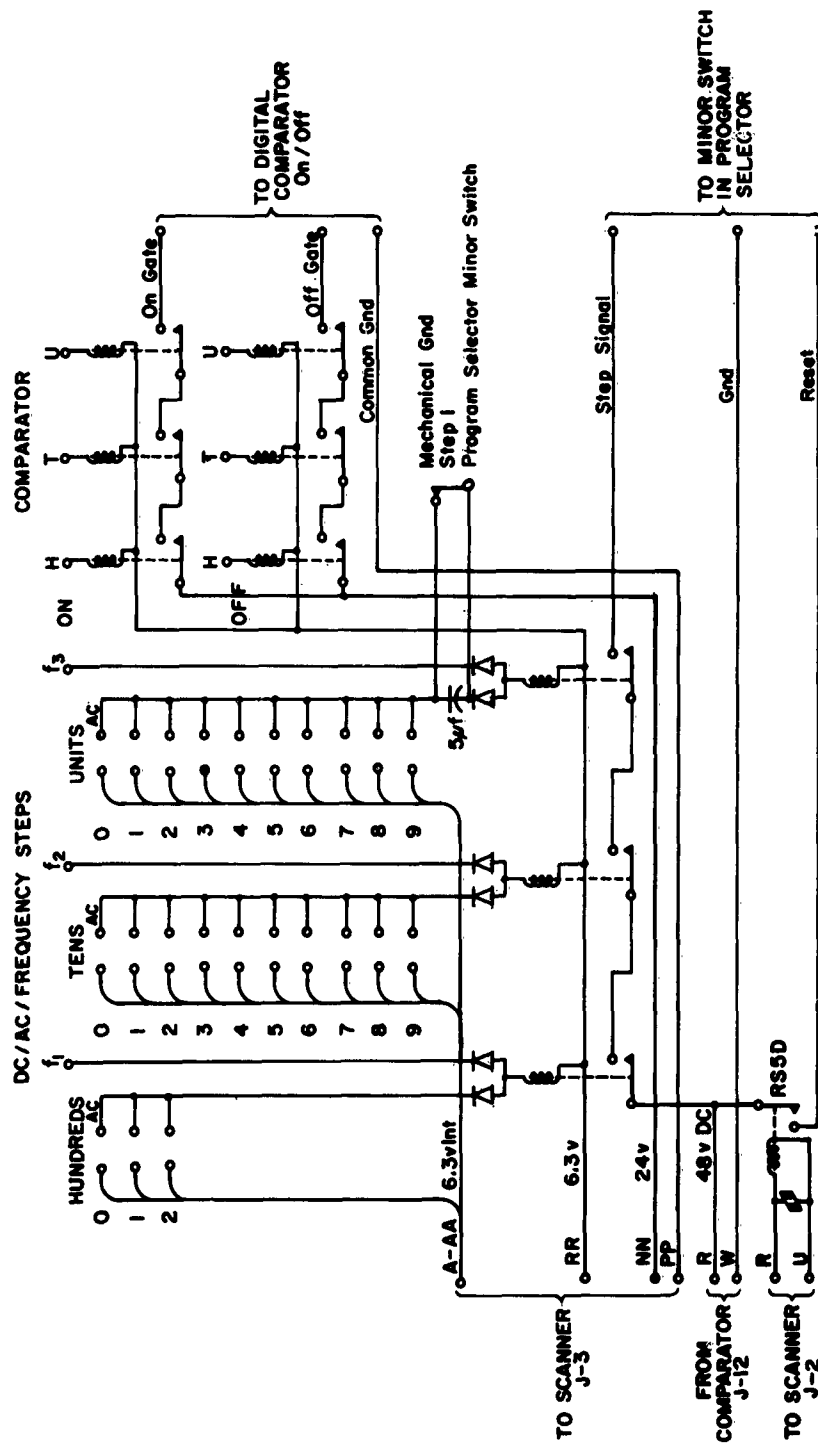
Patch Programmer Front
FIG. 5

Patch Programmer showing Programmer
Relay Banks, Comparator Latching Relay
and Synch. System Relays

FIG. 6

PATCH PROGRAMMER

FIG. 7

All relays except RS5D are ADVANCE, SO SENSITIVE, SO/IC/4000 D
RS5D is P.B. 10,000 Ω, SPDT
All 24V & 48V relays in parallel with VARISTORS of 24V or 48V ratings mfrd. by AUTO ELECTRIC CO.
Use 1N456 glass silicon junction diodes.

switch and causes it to step. The minor switch will step once for AC and once again for frequency. The frequency step is provided by a patch line from the J-3 plug side of the hundreds, tens and units jacks to the jacks marked f_1, f_2, and f_3, respectively. This provides a sequential closing and a second 48 volts is sent to the minor switch. Re-cycling of the program selector is kept in phase with the recycle of the scanner by bleeding recycle voltage directly from the scanner J-2 plug to operate a relay, RS5D, which in turn supplies 48 volts to the reset solenoid of the minor switch. RS5D was determined to be the most expedient means of operation since maximum scanner output is 30 volts and the minor switch requires 48 volts.

The second task of the patch programmer is to turn on and off the digital comparator. When it becomes desirable in an experiment to control with certain of the data — AC, DC, or frequency — the number of the first scanner station to be compared is set in by connecting the J-3 plug side of the patch board hundreds, tens and units jacks through patch cords to the respective hundreds, tens and units jacks of the comparator "on" patch row. A similar procedure is used to turn the comparator off. These patch connections allow the solenoids of the relays to float at 6 volts in the same way as the relays used for stepping the programmer. When a set of three of the comparator relays have closed, 24 volts is sent to the on-off latching relay used in the digital comparator unlocking circuit. The latching relay in turn operates the comparator.

3. The Program Selector routes all inputs in accordance with the patchboard programs. It consists of a gold-plated minor switch which accepts the two line outputs from the scanner. The minor switch is stepped to the DC, AC, and Frequency positions by signals from the patch programmer. The reset signal to the minor switch also comes from the patch programmer and is used in conjunction with the reset of the scanner. This returns the program selector from the frequency position to the DC position. The first two banks of the program selector are used for the two wire inputs from the scanner. The third bank on the minor switch is used to connect either the DC amplifier or the AC-DC
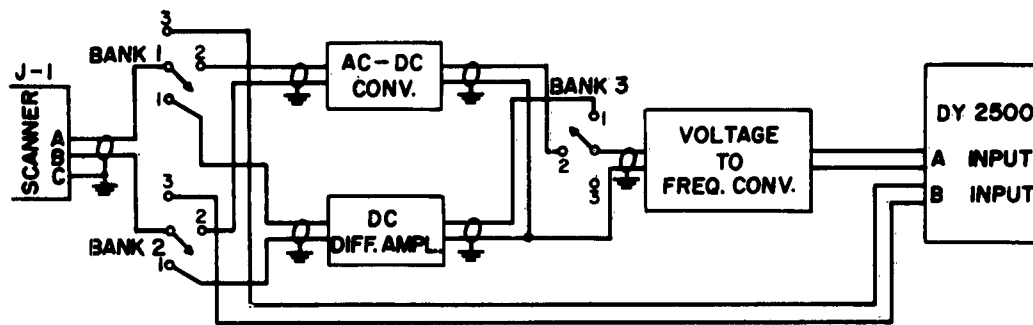
(a)   SIGNAL ROUTING
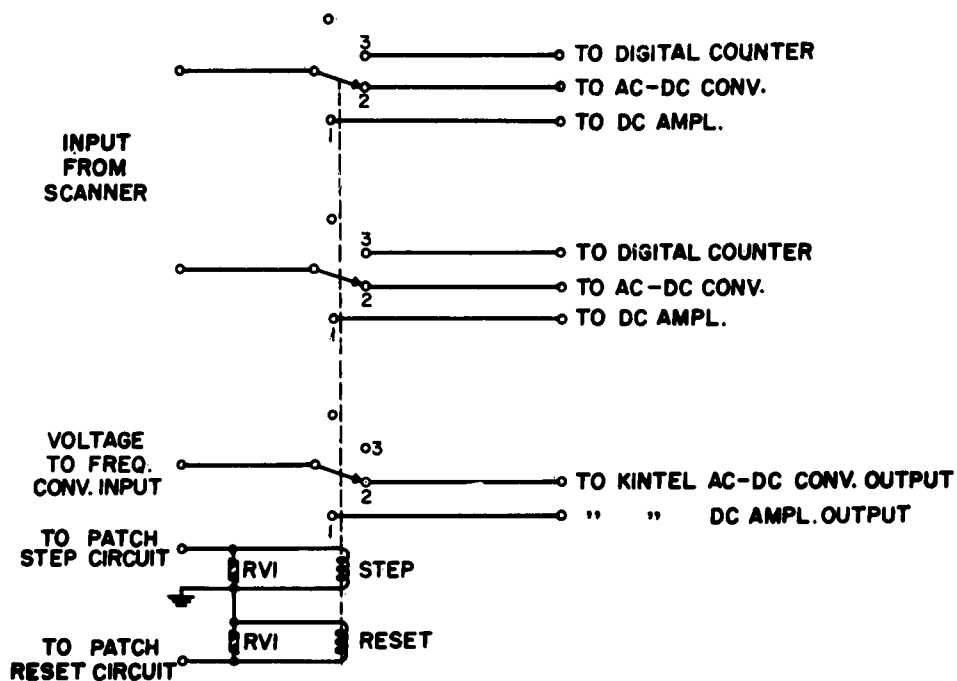
(b) PROGRAMMER MINOR SWITCH

PROGRAM SELECTOR
FIG. 8

converter to the voltage-to-frequency converter. In the frequency position it is unused since frequency is fed directly to the digital counter.

4. The Differential Amplifier is used to amplify microvolt range DC inputs from the DC terminal of the program selector to an appropriate level for accurate counting by the voltage-to-frequency converter.

The amplifier is a Kintel Model 114C floating differential amplifier. It as a gain accuracy of 0.5% and a gain stability of 0.02%. The gain is variable in incremental steps from 10 to 1000.

5. The AC-DC Converter converts AC signal inputs received from the AC terminal of the program selector to corresponding DC voltages suitable for input to the voltage-to-frequency converter.

The model used in this link is a Hewlett Packard 457A. It has an input range of 100 microvolts to 300 volts rms with a 4 decade attenuator range from 1 to 1000. Output range is from 0 to 1.0 volt full scale. Accuracy is 0.3% to 50KC, 0.75% to 500 KC, and where a limited band of input frequency is to be used the AC converter can be tuned to an accuracy of 0.1%.

6. The DC-to-Frequency Converter generates frequencies correspondent to the DC voltage inputs. It is used in conjunction with the frequency counter described in Section 7 because this combination gives the most accurate and versatile analog-to-digital conversion.

The unit used is a Dynmec Model 2211B. It converts a DC input, 0-1.0 volt full scale, to a proportionate frequency, 0 to 100,000 cps full scale. It has an accuracy of ±0.04% and a linearity ±0.002% full scale and ±0.01% of reading. The output wave form is a 5 volt positive pulse of approximately 2.5 millisecond duration.

7. The Digital Counter converts the incoming frequency signal to a 5 digit number signal suitable for acceptance by the printer and the comparator.

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A Dymec Model DY 2500 Computing Digital Indicator is used. It is an electronic counter-timer designed to make rapid, accurate measurements of frequency, period and frequency ratios. Measurements are displayed visually and simultaneously appear as electrical signals. It has a range from 0 to 100KC and an accuracy of ±1 count which for a five digit reading is $\pm 1 \times 10^{-5}$ or ±.001%.

8. The Digital Recorder simultaneously prints the number read by the counter and the number of the scanner station which is being sampled. In addition, it provides an output of any 3 selected digits in analog form for further display by strip chart or galvanometer recorders.

The unit chosen is a Hewlett Packard 560A parallel entry eleven digit recorder. It prints upon manual actuation or automatically upon command from the digital counter. The maximum rate of print is 5 times per second.

Five digits are used for the signal in the counter; 3 digits for the number of scanner station on which the signal appears; and 3 spare digits for experiment identification, elapsed time, or other options desired.

Because it is a parallel entry staircase voltage device, it has an absolute accuracy to the counter to which it is slaved. The analog output is a 1000 step staircase directly proportional to the value of the number printed in any 3 column group selected by a front panel switch.

9. The Ten-Line-to-Staircase Converter is necessary because of the incompatability between the scanner station identification signal and the required form of signal input to the printer. This unit takes a 300 volt source available in the printer and divides it into a set of discrete levels through a string of dropping resistors. The 10 lines for a scanner digit are connected at the appropriate points in the string. The scanner wiper arm which wipes the terminals of these ten lines is then connected through a high impedance to the recorder. This forms, in effect, a voltage divider with the scanner-wiper arm providing discreet levels of voltage for each numeral. Three such circuits are
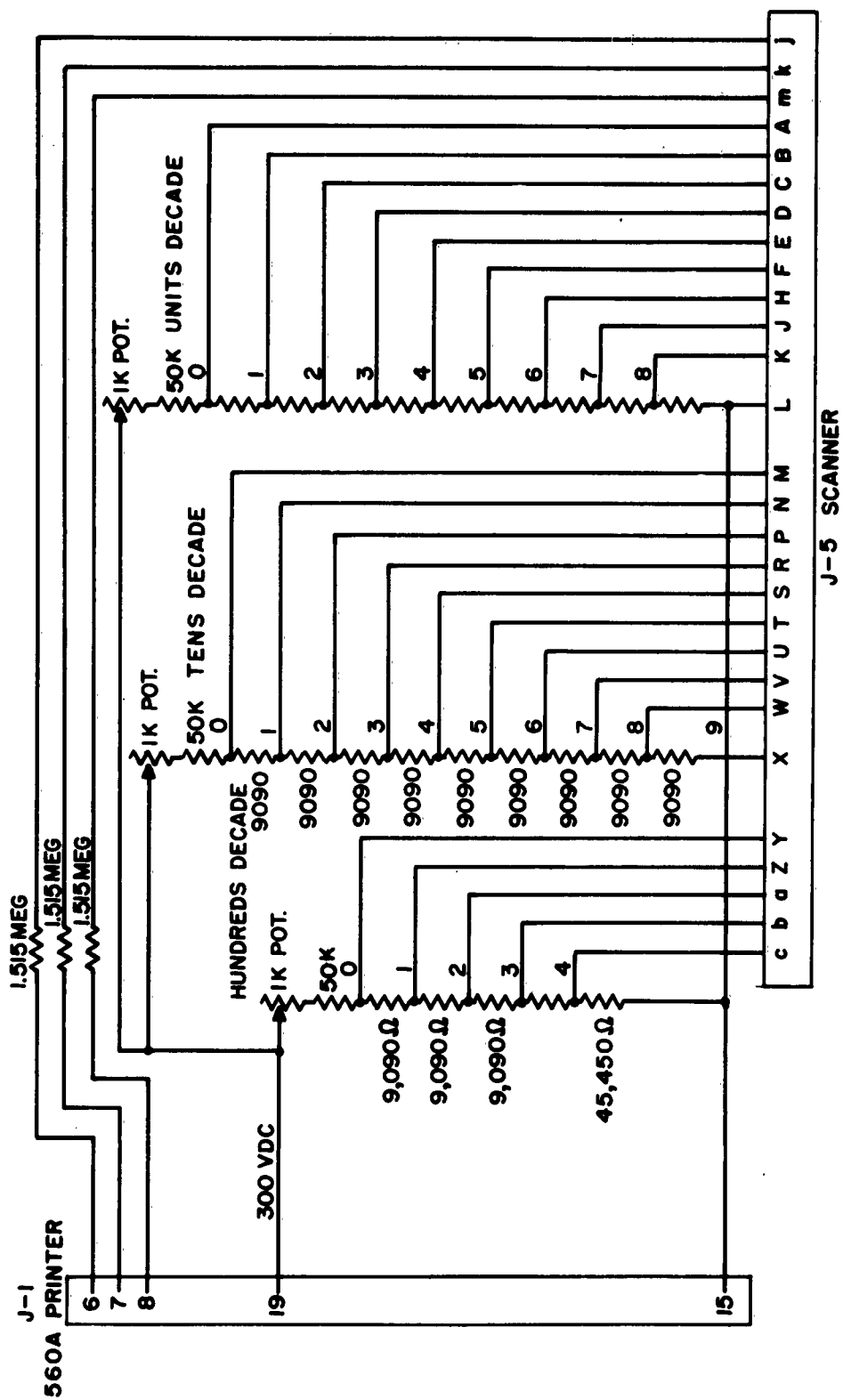
IO LINE TO STAIRCASE CONVERTER

FIG. 9

made: one each for the hundreds, tens, and units digits representing the scanner station number. In order to provide precise voltages and hence insure the proper scanner station number 1% tolerance carbon deposit resistors were used throughout. Calculation of the resistance values was made in accordance with section 2-8 of the Hewlett Packard 560A Operating and Service Manual. Figure 9 shows the wiring and resistance values necessary for the converter.

10. The Binary Decimal Register is is coupling device which transfers parallel digital information from the digital counter to the comparator.

Upon command from the counter the unit, a Dymec DY2530 AR-5 Binary Decimal Register, stores in self-holding relays the binary coded decimal information fed from each of the counters binary counting units. It then transmits this information to the comparator in a 4-2-2-1 binary code. The use of the register between the counter and the comparator is analogous to the function of a buffer storage in a digital computer.

11. The Digital Comparator is used for precise comparison of digital measurements made with the electronic counter against five sequentially selected pairs of preset tolerance limits.

It is a Dynmec DY2538 unit which accepts 4-2-2-1 binary code inputs and matches them through a set of relays with prewired pairs of tolerances. The comparator then indicates whether the signal is above (HIGH), below (LOW), or within (GO) the set limits. This is done through three relays – one for each indication, a relay for each of the five comparison sets, and a set of lights indicating the relay actions. By integrating the relays into a voltage divider system ± error voltages proportionate to the tolerance limits may be obtained and used for control purposes.

12. A System synchronization and Digital Comparator Unlocking Circuit is necessary to turn the comparator on and off and to switch the system synchronization from recorder slaved to comparator slaved.

When the comparator is not comparing, 48 volts from pin R of the comparator J12 connector is routed through a 380 ohm dropping resistor

DY2538/J11

BANK 1

A .1%
B .5%
C 1%
D 5%
E 10%

7 6 5
1 4
2 3

J

Opened at 7 by wiper arm

100 μf

20Ω

BANK2
48v on "Go"

7 6 5
1 4
2 3

Comparator Step

5 μf

DY2538/J12

L J K H F

B
G
C
R
W

48v on "No Go"

48v DC

BANK 3

7 6 5
1 4
2 3

Comparator Reset

330 Ω

380 Ω

560A Printer J-1

20K 240v

20

15

Scanner J-4-T

from Patch

Programmer

Scanner J2-J

2.4 K

SO Sensative
1.6 Ma. Relay
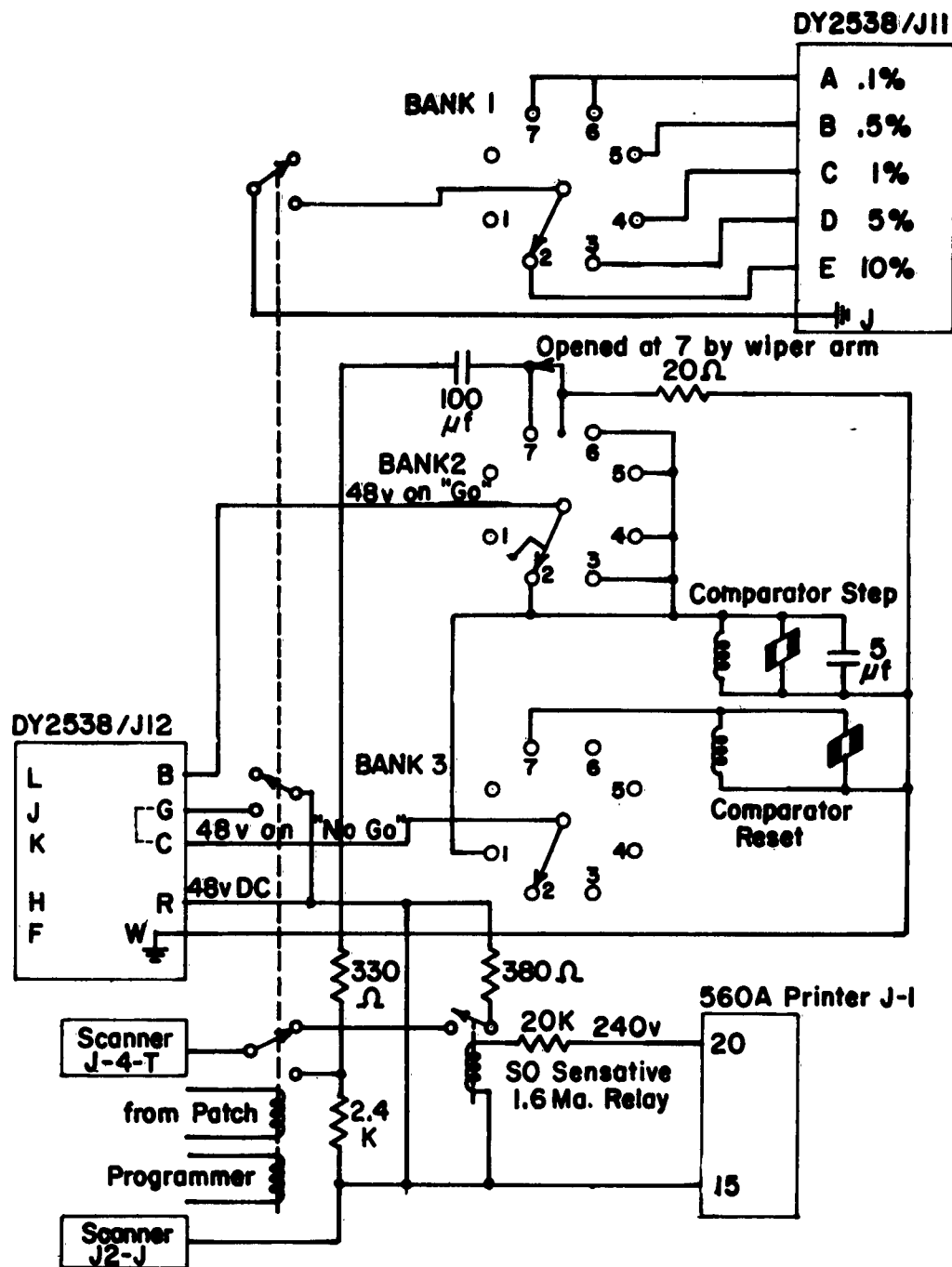
DIGITAL COMPARATOR UNLOCKING GATE, SYNCH SYSTEM,
AND SEQUENCING CKT.

FIG. 10

to the wiper arm of a 1.6 ma "so-sensitive" relay (see Figure 12). Relay closure provides 24 volts across pins J-4-T and J-2-J of the scanner causing it to step to the next input. Operation of the "so-sensitive" relay results from a 240 volt pulse from pin 20 of the 560A printer J-1 plug. This pulse is run through a 20K resistor so that the sensitive relay receives its design current of 1.6 ma. The time required for operation of the scanner stepping relay is incompatible with the short duration of the 240 volt pulse, hence necessitating the sensitive relay. In this mode the 240 volt pulse issued by the printer when it is ready for a new reading momentarily activates the sensitive relay which steps the scanner.

When the scanner reaches the station on which comparator operation is to begin, 24 volts pass through the patch programmer "comparator on" relay contacts and operates the "on-off" latching relay. Turning the latching relay to "on" opens the printer activated scanner stepping circuit and closes the circuit for comparator minor switch operation of the scanner stepping. In this condition when the minor switch reaches position 7, the finest tolerance position, and the signal is within tolerance, 48 volts charges a 100 microfarad condenser thus generating a pulse which passes through a voltage divider and gives the scanner a 24 volts pulse causing it to step. When the comparator reaches the station set for "comparitor-off" on the patch programmer a second series of patch programmer relays close and provide 24 volts to turn the latching relay off. This returns the synchronization system to being printer slaved. The comparison process is turned on or off by routing the grounding line from pin 1 of comparator plug J-11 through one set of the latching relay contacts. When the latching relay is "on" the grounding line is run sequentially via the first bank of the comparator minor switch to the pins causing the energizing of the five tolerance limits. With the latching relay "off" all tolerance relays are deenergized so no comparisons may be made. See Figure 10.

An additional synchronization option may be included to insure no print during recycle. This feature becomes desirable if the scan rate is faster than 1.5 seconds per sample. This option consists of inserting an interrupter relay in the positive print command line to the printer,
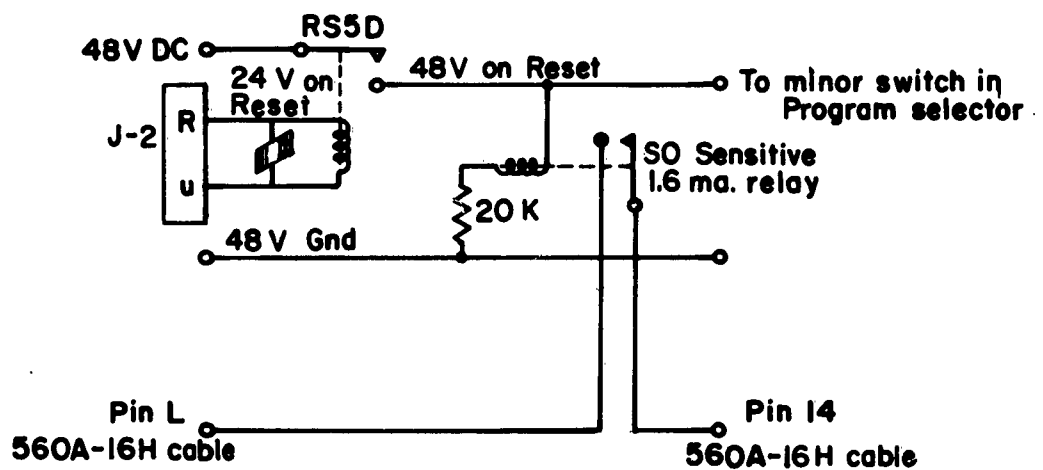
SYNCH SYSTEM OPTION FOR PRINT INTERRUPTION ON SCANNER RESET

FIG. 11

pin L or 14 on cable 560A-16H. This relay is activated by scanner recyle
voltage and would interrupt the print commands during recyle. See ·
Fig. 11.

13. A <u>Comparator Selector Circuit</u> permits digitized signals to
be compared with preset levels in a limit process. Five sequentially
decreasing limits, ±10% tolerance, ±5%, ±1%, ±0.5%, and ±0.1%, are preset
in the comparator. The incoming signal is first compared with the 10%
limit, station 2 on the minor switch. If the signal is larger than the
+10% limit a voltage or closure representing greater than 10% appears at
the output of the comparator and the "HIGH" light comes on. If the
signal is more than 10% below the preselected number a corresponding
negative voltage will appear at the output and the "LOW" light will come
on. If the signal is within the tolerance limits the "GO" light will
come on and the stepping minor switch will then step to the next closer
tolerance lever: ±5%. This process is repeated until the ±0.1% compari-
son reads "GO". This is on station 6. At this point the minor switch
steps once more to station 7. Station 7 is also connected to the 0.1%
tolerance pair and upon reading "GO" again the scanner steps to the
next station. The minor switch then recycles and the comparison process
starts again for the next signal at the 10% tolerance level.

Control voltage is supplied by plus and minus 48 volts to pins J
and F respectively of plug J-12 of the comparator. This voltage
is then fed through a relay bank and voltage dividers to give error
signals proportional to the prescribed tolerance limits. See Fig. 12.

14. The <u>Digital Comparator Stepping and Recycle Circuit</u> makes the
comparator capable of stepping down the tolerance staircase. In addi-
tion it provides the comparator minor switch reset logic and scanner
step actuation when the comparator latching relay is "ON". See Fig. 10.

With the minor switch on position 1 no comparison is made. The
"GO" solenoid in the comparator is deenergized, i.e., in the "NO GO"
position and supplies 48 volts through the "NO GO" wiper arm to pin 1
of bank 3 of the minor switch. Pin 1 of bank 3 is connected to the
stepping relay so the minor switch steps to position 2 and the first

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BANK I

48V., 10 POLE
COMPARATOR
MINOR SWITCH

J11 of DY 2538

A (.1)
B (.5)
C (1%)
D (5%)
E (10%)
J

LATCHING RELAY

(a)   COMPARATOR SELECTOR CKT

J12 of DY 2538

To pos. 48V Bat.   F   W
1   .48V   495K   A   K
                                               L
2   2.4V   476K   B   M
                                               N
3   4.8V   450K   C   P
                                               Q
4   24V   250K   D   S
                                               T
5   48V   E   U
                                               V
                                               D
                                               H
5K   24K   50K   250K   500K   J
                                               A
6   E
−48V   F
                    +48V DC   R

(b)   ERROR SIGNAL GENERATOR

FIG. 12

- 25 -
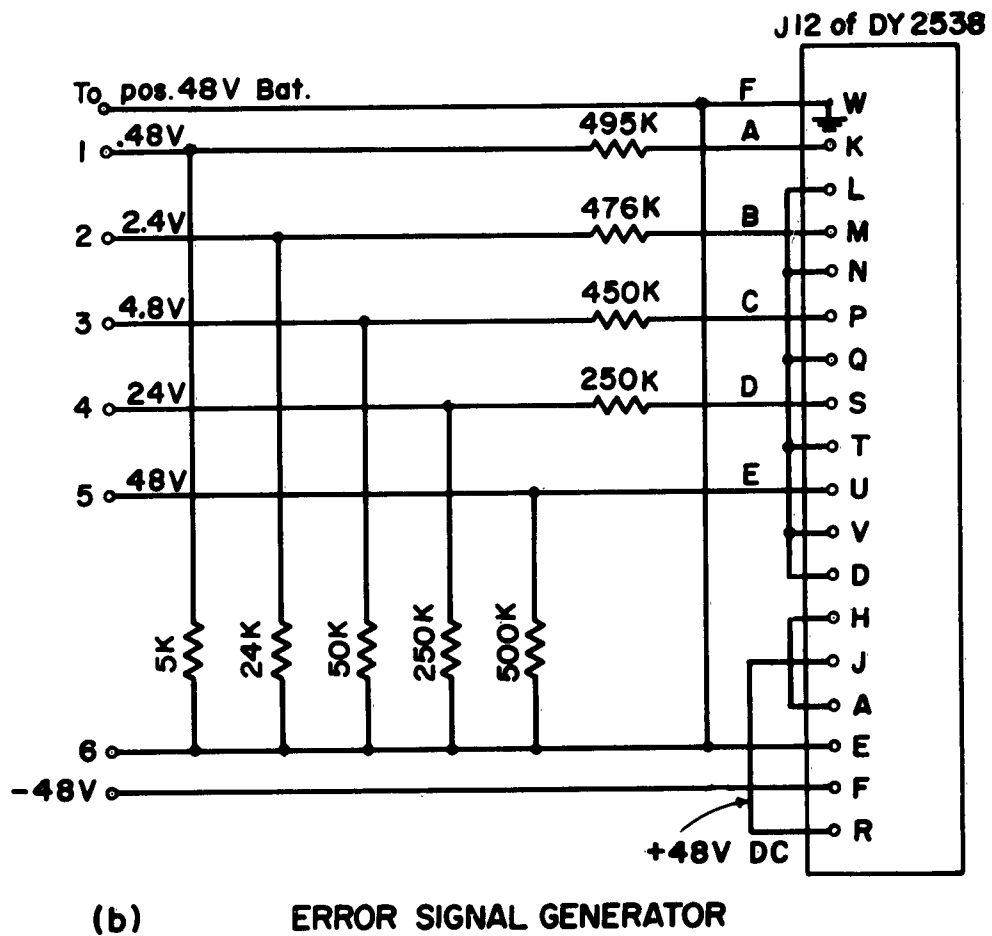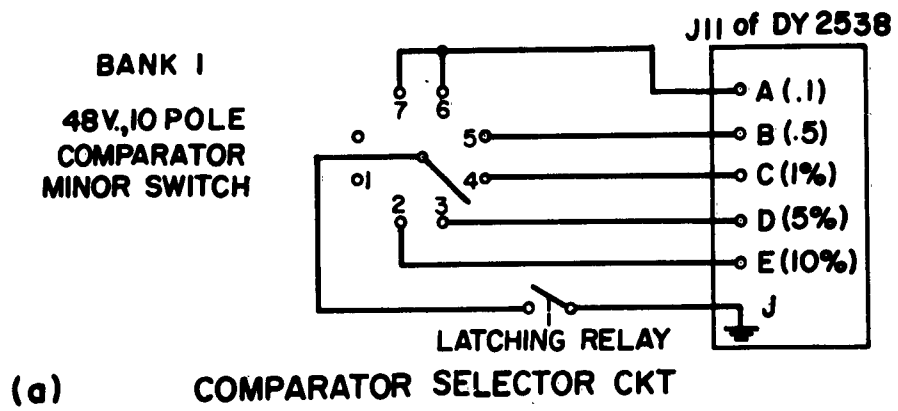
comparison (±10%) is made. Pin 2 through 6 of the third bank of the minor switch are disconnected hence "NO GO" voltage will not step the minor switch in these positions. "NO GO" position 1 was necessary due to the time constant for capacitor discharge in the scanner step circuit.

When the minor switch is on position 2, a unique output voltage will be generated if the absolute value of the comparison error is greater than 10%. When the control voltage has driven the device so that the absolute value of the error is within the 10% tolerance limits, the "GO" relay is pulled in and 48 volts appears on the wiper arm of bank 2 of the minor switch. This steps the minor switch to position 3 and a 5% comparison is made. The process is repeated until the control voltages have driven the parameter being sampled to within the ±0.1% tolerance limits. This occurs on position 6. Forty-eight volts "GO" voltage on wiper arm 2 steps the minor switch to position 7. Position 7 is also wired to the 0.1% tolerance limit and since "GO" was on 6 it will be on 7 also. Pin 7 of bank two of the minor switch is attached to a 100 mfd condenser and then through a voltage divider and latching relay contacts to the pulse-driven stepping relay on the scanner. The 100 mfd condenser changes the 48 volts to a broad pulse which is reduced to a 24 volt magnitude and sent to the scanner, stepping it. When the scanner steps the comparitor "GO" is released and the "NO-GO" voltage appears on wiper arm 2, passes through pin 7 of bank 3, and resets the minor switch to position 1.

Program   Comparator
Selector   Tolerance Sequencing   IO Lines to DC Converter
                    Circuit

Error Signal
Network

Comparator
off Relays

Comparator
on Relays

Synchronization   Patch Programmer
   System
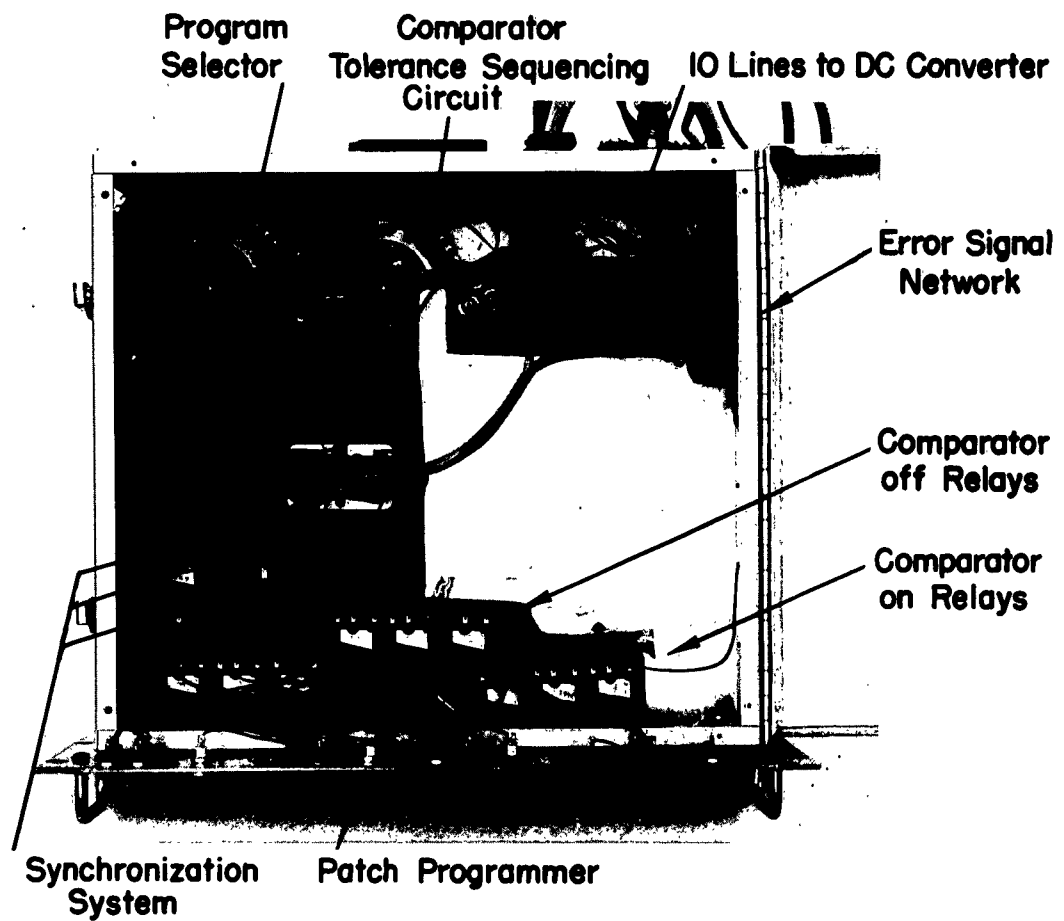
Chassis Containing Patch Sub System Components

FIG. 13

V. SYSTEM PERFORMANCE

The data acquisition system will accept 200 2-wire inputs. These are divided into 100 unshielded and 100 shielded pairs. The division was made arbitrarily and was based upon the estimated ratio of DC to AC and frequency inputs. All inputs were not shielded because of the ensuing congestion in the scanner terminal compartment. It was decided that 100 shielded pairs would contain a safe capacity margin for our requirements. The only restrictions with regard to input location are that the last input shall be prior to scanner station 201, and all similar types of signal shall be grouped together. Gaps are permitted except in comparator ranges. In this case if stepping is external-signal controlled, a gap will cause scanning to stop. In all other cases it serves as a most useful device either to separate types of input or to act as a check station.

Sampling out of sequence is possible and can be most easily achieved by attaching the desired pair to more than one input terminal. For example, one important signal may be attached to 0, 5, 10, 15, ... so as to be monitored every fifth station while the remainder of the lines continue to be monitored once each cycle. Many permutations may be made in this vein to suit the requirements of the particular test.

Another variation which may be achieved is the short recycle. Conditions may arise, for example, where it is desirable to sample 50 signals, 40 of which are initial conditions or change very slowly and 10 of which require close observation. Put the static pairs in the first 40 input lines (000-039) and the dynamic ones in the last 10 (040-049) set recycle on 049 and start on 000. Reset the scanner manually to 000. Now change the start dials to 040 but do not reset the scanner. When the system is turned on the scanner will take the first scan from 000 through 049 and then make a short recycle to 040 and continue resampling the last ten inputs. Variations on this can be easily made and start and stop numbers can be changed during the scanner operation if desired.

During comparator operation the stepping of the scanner occurs only after the particular station being sampled has its input driven to within 0.1% of the preset reference. Should it become desirable to move on to a subsequent station without undue delay and before the 0.1% tolerance has been achieved, this can be accomplished by setting the scanner selector on "internal" and adjusting the time delay on the scanner for the desired period. In this mode if the signal is still out of tolerance at the end of the delay period (3-15 seconds) the scanner will automatically step to the next station.

An even faster stepping may be achieved by jumpering the contact on the latching relay so that the scanner will always step upon command by the printer. However, the comparator will not function efficiently as a controller in this case.

In the course of a scanning cycle, it may become desirable to operate the comparator more than once during a cycle. Allowance has been made to do this provided not more than one column of digits is changed: e.g. "ON" at 053 "OFF" at 062 "ON" at 073 "OFF" at 092. Here only the tens column has been changed.

As has been stated before the maximum rate of sampling depends on the recorder in the "comparator off" mode and on the response of the sampled parameter in the "comparator on" mode. When operating at less than maximum rate, 0.2 seconds, the sampling speed is controlled by adjusting the display time dial on the digital counter. This dial may be set from 0 to ∞. Varying the display time above 0.2 seconds directly regulates printing by the digital printer and hence governs the scanner stepping rate. The display time may be varied during a scanning cycle, if desired, and will in no way affect the accuracy of the system.

The overall system accuracy is a function of both the type of input: frequency, DC and AC, and of the time base of the digital counter. The accuracy of the counter is ±1 count. Thus for a 1 volt equivalent input counted for 1 second we have a reading of 10,000 ±1, an accuracy of 1×10^{-4}. For the same signal sampled for 10 milliseconds we read

100 ± 1, an accuracy of 1%. In the following calculations we assume use of a 1 second count time and a counter input signal equivalent to several hundred millivolts.

a. Frequency inputs

Digital Counter Accuracy: $±1 \times 10^{-4}$

Overall Accuracy: 99.99%

b. DC Inputs

DC Differential Amplifier   ±0.52%

Voltage to Frequency
  Converter   ±0.04%

Digital Counter   ±0.01%

Overall Accuracy   99.43%

c. AC Inputs

AC-DC Converter   ±0.3% (nominally)

Voltage to Frequency
  Converter   ±0.04%

Digital Counter   ±0.01%

Overall Accuracy   99.65%

It should be noted that the comparator and the recorder do not enter the accuracy considerations for the system since they achieve absolute accuracy to the counter.

Figure 14 shows samples typical of mixed data taken during a test run. The sampling rate was 2 stations/second. Stations 000 through 009 were DC inputs; 010 through 014 were AC; and, 015 through 020 were frequency. The comparator was operated on station 005; and, as can be seen, the scanner remained on station 005 until the control voltages drove the signal to within ±0.1% of 1000 (1.0 volt). The first 3 digits on the left are the scanner station number; the next five are the data. The blank space on the left of the tape is where the 3 additional columns may be printed if timing or other options are desirable. Figure 15 shows the stepped control voltage corresponding to the tolerance levels reached as shown on the adjoining tape.

Inputs

Frequency

AC

DC

Comparator operation on 005

```
0 2 0 0 0 5 0 0
0 1 9 0 0 3 0 1
0 1 8 0 1 5 3 2
0 1 7 0 0 4 0 9
0 1 6 0 0 8 2 3
0 1 5 0 0 5 5 3
0 1 4 0 0 0 0 1
0 1 3 0 0 0 4 8
0 1 2 0 2 8 9 1
0 1 0 0 0 0 2 2
0 1 0 1 3 5 3 9
0 0 9 1 4 1 8 3
0 0 8 0 2 6 4 1
0 0 7 0 2 6 4 1
0 0 6 0 2 6 4 1
0 0 5 0 9 9 9 1
0 0 5 0 9 9 7 1
0 0 5 0 9 9 5 5
0 0 5 0 9 8 7 2
0 0 5 0 9 8 4 2
0 0 5 0 9 7 8 4
0 0 5 0 9 6 4 8
0 0 5 0 9 5 6 1
0 0 5 0 9 4 9 7
0 0 5 0 9 3 9 4
0 0 5 0 9 2 7 8
0 0 5 0 9 1 8 2
0 0 5 0 9 0 9 4
0 0 5 0 8 9 2 6
0 0 5 0 8 9 3 5
0 0 4 0 1 3 2 5
0 0 3 0 1 3 3 4
0 0 2 0 1 3 1 2
0 0 1 0 1 3 4 8
0 0 0 0 2 6 6 2
```

3 blank columns

Scanner station number

Transducer signal value

Output Typical of Mixed Data Run
FIG. 14
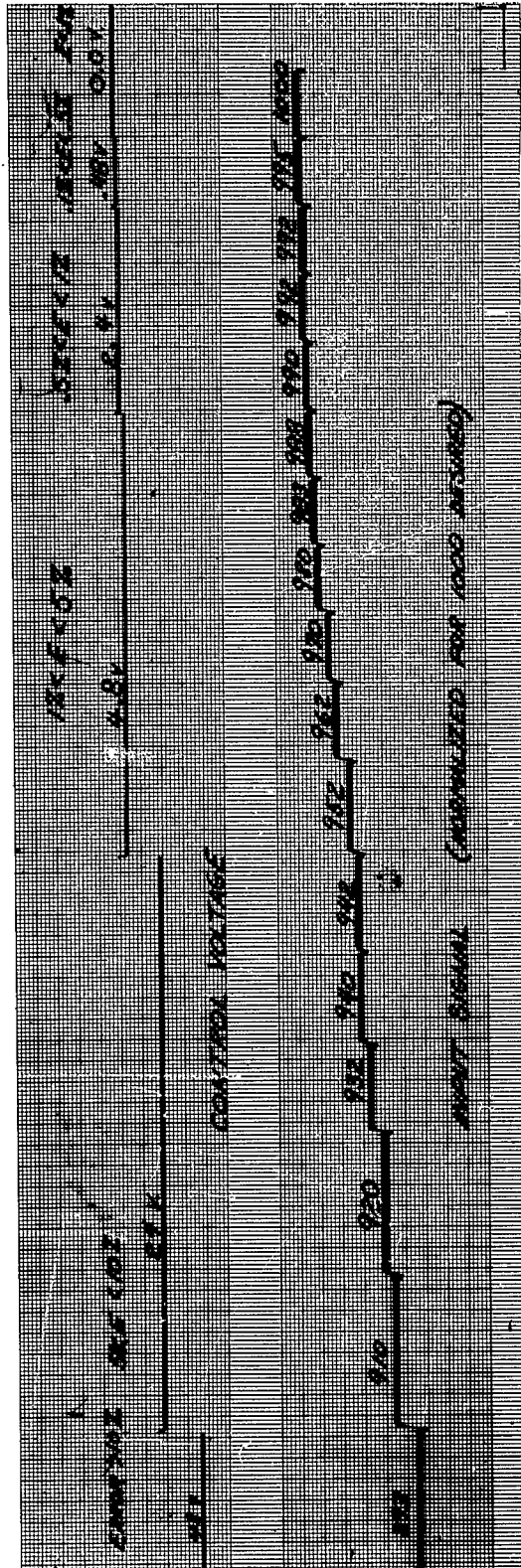
Control Voltage vs Input Signal

FIG. 15

SUMMARY AND CONCLUSIONS

This paper presents a design for an inexpensive, mobile, accurate, broad spectrum data acquisition system with digital readout and control capability. It will accept the outputs from a wide range of common transducers, scan them at a rate up to 5 per second, and process them to an overall accuracy of at least 99.43%.

The detailed study of the various components used in the synthesis of the system revealed that it is feasible to extend both the scope and versatility of operation, e.g., both integration and differentiation seem capable of accomplishment. One avenue worthy of immediate exporation is the apparent ability of the computing digital indicator to differentiate a given function to a most high degree of accuracy. It is strongly recommended that such a possibility be given further consideration.